

Job offer

INTERNSHIP

Evaluation of an High Level Synthesis Flow applied to NanoXplore FPGAs

We are seeking a motivated intern to evaluate and optimize a High-Level Synthesis (HLS) design flow for NanoXplore FPGAs. This role focuses on exploring how HLS tools can accelerate FPGA development by converting high-level descriptions (e.g., C/C++) into efficient hardware implementations. The intern will benchmark the HLS flow against traditional RTL approaches, analyze performance, resource utilization, and timing results, and propose improvements tailored to NanoXplore's FPGA architecture. This project offers hands-on experience with advanced FPGA technologies, synthesis methodologies, and performance analysis in a real-world industrial context

Your missions

- Investigate and implement HLS-based design flows for NanoXplore FPGAs.
- Benchmark HLS-generated designs against RTL implementations in terms of performance, resource usage, and timing.
- Analyze synthesis reports and identify optimization opportunities.
- Propose and validate improvements to enhance efficiency and compatibility with NX FPGAs
- Document findings and present recommendations to the technical team.

Profile

- Currently enrolled in a Master's program in Electrical Engineering, Computer Engineering, or related field.
- Strong knowledge of FPGA design principles and digital logic.
- Familiarity with C/C++ programming and hardware description languages (VHDL/Verilog).
- Understanding of synthesis tools and design flows (HLS experience is a plus).
- Analytical mindset and ability to interpret performance metrics.
- Basic scripting skills (Python) for automation.

Duration & Location

- Internship
- Location : Sèvres (92)
- Start Date : 2026 (Q1 or Q2)

Excited by this role ? We'd be happy to hear from you !

Send your CV at : careers@nanoxplore.com